

**Remarks**

Claims 1-24 were presented in the application filed August 22, 2001. In the present office action, the Examiner has rejected claims 1-24. By this amendment, claims 21 and 23 have been canceled, and claims 1, 3, 5, 6, 9-17, 20, 22, and 24 have been amended. Thus, claims 1-20, 22 and 24 remain in this application.

The examiner rejected claim 5 under 35 USC §112 because it contained an improper dependency. Applicant has amended claim 5 according to the examiner's assumption.

The examiner rejected claims 1, 3, 4, 6, 9, 10-12, 14, 15, 17, 18 and 21-23 under 35 USC §102(b) as being anticipated by Hirata et al., US Patent No. 5,056,058. Before an analysis of the examiner's rejections of specific claims is undertaken, a brief overview of Hirata, vis-à-vis the present invention is considered relevant.

Hirata teaches prediction of communication between a first communication control equipment and a second communication control equipment within a predetermined communication protocol [see Abstract, lines 2-5]. That is, Hirata presumes a particular communication protocol (such as TCP/IP), and then predicts a next TYPE of communication between the first communication control equipment, and the second communication control equipment, based on the previously transmitted frame [see Abstract lines 5-10]. The TYPE of communication that is predicted is Data Transfers versus Acknowledgements [see Figure 5 and associated text]. Hirata thus presumes a defined protocol, and frame specifics such as the source of transfer, the destination of transfer, the size of the transfer etc. That is, Hirata already knows that the protocol is fixed. And, Hirata knows what the source and destination of a packet is. All that Hirata predicts is whether the next frame between a source and a destination is another transfer frame, or an acknowledgement, as well as a few other TYPES of communication within the fixed protocol.

In contract, Applicant's invention DOES NOT presume a source, a destination, a size, a protocol, or any other attribute about a packet, NOR is applicant concerned about predicting the TYPE of frame (i.e., data transfer versus acknowledgement). Rather, Applicant is concerned about predicting information within specific packets, received from many different sources, and destined for many different destinations, having varying sizes of transfer, and using different protocols (UDP, TCP/IP, etc.). That is, it is not the TYPE of frame that is being predicted, but the specific information within packets that is necessary for ROUTING of the packets between sources and destinations, such as must be performed by routers. More specifically, Routers receive packets from thousands of different sources, destined for thousands of destinations, of varying sizes, and of different protocol. All of the information within each packet received by a router must be processed, to determine its origin, its destination, its size, its protocol, etc. It is the prediction of this information, and the processing of this information, to reduce latency typically associated with processing after packets are received to which the present invention is directed. Nothing in Hirata teaches, suggests, or even hints at this novel invention.

With respect to claim 1, it is repeated below, as amended, for ease of reference:

1. (currently amended) A packet buffering system for predictively processing data packets in a data packet network comprising:
  - at least one input port for receiving data packets from a plurality of sources;
  - at least one output port for sending out data packets to a plurality of destinations;
  - a packet predictor, coupled to said at least one input port, for predicting information about a future packet based on history of a previously received packet;
  - a plurality of queues for storing packets received from said plurality of sources, and for storing said predicted information about said future packet; and
  - a processing core, coupled to said plurality of queues, such that at least some processing for said future packet may be accomplished before said future packet actually arrives at the system.

Nothing in Hirata teaches an input port for receiving data packets from a plurality of sources (Hirata must know the source of a frame); one output port for sending out data packets to a plurality of destinations (Hirata must know the destination of a packet); a plurality of queues for storing predicted information about a future packet (Hirata teaches predicting the TYPE of communication (transfer, acknowledge, etc.) NOT the information within a packet that defines source, destination, protocol, size, etc.); or a processing core for processing predicted information about a future packet. In view of the foregoing amendment, and the clarifications between Hirata and the present invention, application respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 2-8, these depend either directly or indirectly from claim 1 and add further limitations that are neither anticipated nor obviated by Hirata. For all of the above reasons, applicant respectfully requests the examiner to withdraw his rejections of these claims.

With respect to claim 9, it is repeated below as amended for ease of reference.

9. (currently amended) A packet predictor system for predicting information about a future packet to be received within a data packet processor, the predicted information being processed by a processing core prior to the future packet being received, the processing reducing latency in routing the future packet to its destination, the system comprising:

- an input for receiving information about a first packet received for processing;

- a packet predictor, coupled to said input, for predicting the information about the future packet, based upon the information received about the first packet;

- a plurality of queues, coupled to said input and said packet predictor, for storing the predicted information; and

- a processing core, coupled to said plurality of queues, for processing the predicted information before the future packet is received by said input;

wherein by processing the predicted information before the future packet is received, latency for delivering the future packet to an output is reduced.

As mentioned above with respect to claim 1, nothing in Hirata teaches a packet predictor for predicting information about a future packet (Hirata predicts the TYPE of transaction, and information about the packet); a plurality of queues for storing the predicted information; or a processing core for processing the predicted information before the future packet is received. For these reasons, and for those stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 10-16, these depend from claim 9 and add further limitations which are neither anticipated nor obviated by Hirata. For all of the above reasons, application respectfully requests the examiner to withdraw his rejections of these claims.

With respect to claim 17, it is repeated below as amended for ease of reference:

17. (currently amended) A method for reducing latency in packet processing within a packet processor, comprising the steps of:
  - receiving packets from a plurality of sources;
  - developing and storing a history of packet information from the received packets;
  - predicting future information about future packets from the history; and
  - processing the future information about the future packets before the future packets are received;

wherein by processing the future information about the future packets before the future packets are received, latency in delivering the future packets to their destinations is reduced; and

wherein the information comprises one or more of packet type, packet flow identification, source information, destination information, and packet size.

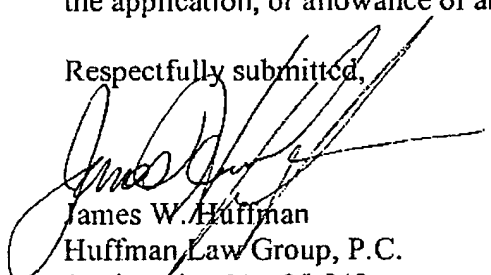
Hirata does not teach, suggest or even hint at the steps of receiving packets from a plurality of sources, developing a history of packet information from the received packets, predicting future information about future packets from the history, and processing the future information. For these reasons, and for those stated above with respect to claims 1 and 9, applicant respectfully requests the examiner to withdraw his rejection of this claim.

With respect to claims 18-20, 22, and 24, these depend either directly or indirectly from claim 17 and add further limitations that are neither anticipated nor obviated by Hirata. For all of the reasons stated above, applicant respectfully requests the examiner to withdraw his rejection of these claims.

With respect to claims 21 and 23, these have been canceled thereby rendering rejections of those claims moot.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

Respectfully submitted,

  
James W. Huffman  
Huffman Law Group, P.C.  
Registration No. 35,549  
Customer No. 23669  
1832 N. Cascade Ave.  
Colorado Springs, CO 80907  
719.475.7103  
719.623.0141 fax  
jim@huffmanlaw.net

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